CALIFORNIA STATE UNIVERSITY, FULLERTON

Computer Engineering

EGCP 520 – Advanced Computer Architecture (Fall 2016)

Homework no 4 (Due date: October 26, 2016 midnight (11:55 pm))

1. (16 Points) Pipelining

An unpipelined processor takes 8 ns to work on one instruction. It then takes 0.2 ns to latch its results into latches. I was able to convert the circuits into 8 sequential pipeline stages. The stages have the following lengths: 0.8ns; 1.2ns; 0.7ns; 1.4ns; 0.8ns; 0.4ns; 1.4ns; 1.3ns. Answer the following, assuming that there are no stalls in the pipeline. **Show your work to receive full credit.**

a. What are the cycle times in both processors (in nano-seconds)?
b. What are the clock speeds in both processors (in MHz)?
c. What are the IPCs in both processors?
d. How long does it take to finish one instruction in both processors (in nano-seconds)?
e. What is the speedup provided by the 8-stage pipeline?
f. If I was able to build a magical 1000-stage pipeline, where each stage took an equal amount of time, what speedup would I get?

2. (10 Points) Data Dependencies

Consider a 32-bit in-order pipeline that has the following stages. Note the many differences from the examples in class: a stage that converts CISC instructions to micro-ops, two stages to do register reads and writes, two stages to access the data memory, and 3 stages for the FP-ALU (floating-point ALU). For the questions below, assume that each CISC instruction is simple and is converted to a single micro-op.

Fetch	Covert to μ-ops	Decode	Regread	Regread	IntALU	Regwrite	Regwrite		
					IntALU	Datamem	Datamem	Regwrite	Regwrite
					FPALU1	FPALU2	FPALU3	Regwrite	Regwrite

After the instruction fetch, the instruction goes through the micro-op conversion stage, a Decode stage where dependencies are analyzed, two Regread stages where input operands are read from the register file. After this, an instruction takes one of three possible paths:

1. Integer adds (Int-adds) go through the stages labeled "IntALU" and 2 "Regwrite" stages.
2. Loads/stores go through the stages labeled "IntALU", "Datamem", "Datamem", "Regwrite", and "Regwrite".
3. Floating-point adds (FP-adds) go through the stages labeled "FPALU1", "FPALU2", "FPALU3", "Regwrite", and "Regwrite".

Assume that the register file has an infinite number of write ports so stalls are never introduced because of structural hazards. How many stall cycles are introduced between the following pairs of successive instructions (i) for a processor with no register bypassing and (ii) for a processor with full bypassing?

a. Int-add, followed by a dependent Int-add
b. FP-add, followed by a dependent load
c. Load, providing the address for a store
d. Load, providing the data for a store
e. FP-add, providing the data for a store